National Institute of Electronics and Information Technology (NIELIT)
Dwarka, New Delhi

राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान, द्वारका, नई दिल्ली -110077

DETAILED ADVERTISEMENT
(Advt. No. NHQ-12/412025-NIELIT/3169108)

NIELIT requires the following person purely on contract basis on consolidated remuneration initially for a period of one year: -

1. Name of Position	Resource Person (Academic-Operations)
Position Code	**2512-RPAO**
No of Position	01 (one) NIELIT Corporate Office
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Upto 35 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	₹50,000/- per month
Eligibility Criteria and Experience	**Education Qualification:** Post Graduate in any discipline **Experience:** - 2 Years of post-qualifications experience in Academics & skilling. **Job Description:** Key responsibilities include: Stakeholder Management: Coordinate with key stakeholders, including educational institutions, industry partners, and regulatory bodies, to enhance collaborative partnerships, Working with Skilling Portal: Good Understanding of working with Skilling Portal, Document Management: Support the creation and maintenance of comprehensive documentation for academic standards and qualifications, Management of Data. Reading and grasping reports prepared by Government entities.
2. Name of Position	**Consultant (**DFT and FPGA Validation**)**
Position Code	**2512-CONSDFT**
No of Position	**1 (One),** Hybrid (Remote with Minimum 8 days onsite presence per Months.
Tenure/ Period	Initially for 6 Months (purely on contract basis) but may be extended depending on their performance and budget availability under the project.
Age Limit	Upto 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 2.50 Lakhs per P.M
Eligibility Criteria and Experience	• B.E./B.Tech/M.Tech in Electronics, VLSI, or related fields • Minimum 6-10 years of experience in VLSI industry **Scope of Work:** • Development of high-quality DFT training content and demonstration modules. • Creation of reusable reusable DFT integration examples and mini-projects at IP and SoC levels • Lead FPGA-based test structure validation and post-synthesis debugging. • Mentor learners and faculty contributors in DFT principles and flow automation. **Deliverables:** • 10+ hours of DFT and FPGA validation lecture content. • 4–6 reusable DFT test structures and integration scripts. • 2–3 FPGA-based validation modules demonstrating post-scan testing.

	• Complete documentation and reference design examples. • Monthly progress reports and review presentations. • Support in certification and learner evaluation materials
3. Name of Position	**Consultant (**Physical Design **)**
Position Code	**2512-CONSPD**
No of Position	1 **(One),** Hybrid (Remote with Minimum 8 days onsite presence per Months.
Tenure/ Period	Initially for 6 Months (purely on contract basis) but may be extended depending on their performance and budget availability under the project.
Age Limit	Upto 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 2.50 Lakhs per P.M
Eligibility Criteria and Experience	• B.E./B.Tech/M.Tech in Electronics, VLSI, or related fields • Minimum 6-10 years of experience in VLSI industry **Scope of Work:** • Development of physical design–related lecture content and hands-on laboratory sessions. • Development reference physical design flows, reusable scripts, and example layouts for educational use. • Implementation and validation of design blocks through floorplanning, placement, CTS, routing, and timing analysis. • Providing mentorship and quality assurance for physical design materials and learner submissions. • Lead in certification processes and the creation of evaluation tasks focused on physical design concepts and debugging. **Deliverables:** • **10+ hours of recorded PD lecture content**, including slides and instructor notes covering all major stages of the physical design flow. • **3-5 complete physical design reference projects** demonstrating floorplanning, placement, CTS, routing, extraction, and timing analysis, with reproducible scripts and results. • **A standardized PD flow script package** containing TCL/Python/Makefile-based automation for key implementation stages, along with configuration templates. • **Hands-on lab modules** (10+ labs) with guided instructions, input design files, expected outputs, and troubleshooting notes. • **Documentation bundle** covering design methodologies, tool usage steps, timing interpretation, and layout checks suitable for integration into the EdTech platform. • **Monthly progress reports and review presentations** summarizing completed work, issues, tool improvements, and upcoming tasks.
4. Name of the Position	**Team Lead (VLSI Design)**
Position Code	**2512-TLVD**
No. of Position	**05**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly)	Rs. 95,000/- P. M.

(inclusive of statutory compliances, if any) [CTC]	
Eligibility Criteria and Experience	**Essential:** Bachelor's/Master's/PhD in Electronics & Communication Engineering, VLSI Design, or related field. **Experience:** 4 years of relevant experience in industry/academia/R&D Organization **Note:** Duration of PhD will be counted as R&D experience **Job description:** Key responsibilities include: • Lead the design and development of reusable IP blocks using open-source EDA tools, and oversee their validation and documentation • Drive end-to-end ASIC/SoC design workflows using open-source EDA tools, and coordinate benchmarking of developed IPs and ASICs/SoCs against results from closed-source EDA tools to ensure performance, area, and power metrics are industry-comparable • Lead a cross-functional team for content creation, tool integration, and platform delivery. • Design and develop audio-visual content and labs for RTL-to-GDSII flow using open-source EDA tools. • Oversee integration of open source EDA tools and design flows into the web-based EdTech platform. • Collaborate with academic and industry experts to develop and update modular, job-ready curricula. • Mentor junior engineers and trainers; drive knowledge sharing and skill development. • Facilitate community-building, including forums, bootcamps, and mentorship initiatives. • Ensure quality, track learner feedback, and implement continuous improvements in training and platform features. **Preferred Skills** • Strong understanding of instructional design principles and curriculum frameworks (AICTE, NEP, etc.). • Familiarity with LMS platforms (e.g., Moodle, Canvas) and digital content formats (SCORM, MP4, PDFs). • Experience working with academic institutions or government skilling programs. • Excellent organizational, communication, and mentoring skills.
5. Name of the Position	**VLSI Design Expert/ Junior VLSI Engineer**
Position Code	**2512-VLSIDE**
No. of Position	**04**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 40,000/- P.M
Eligibility Criteria and Experience	**Essential:** Master's/PhD in Electronics & Communication, Electrical Engineering, VLSI Design, or related field. **OR** Bachelor in Electronics & Communication, Electrical Engineering, VLSI Design, or related field with one year's experience **Job description:** Key responsibilities include: • To assist in design and development of reusable IP blocks

	using open-source EDA tools, their validation and documentation
	
	• Design and develop in-depth academic and practical content in one or more of the following domains:
	  o **RTL Design & Integration**
	  o **Physical Design**
	  o **Synthesis and STA**
	  o **DFT and ATPG**
	  o **Analog and Mixed-Signal Design**
	  o **Digital and Analog Design Verification**
	  o **Standard Cell and PDK-based design**
	• Create reproducible design labs and projects using open-source tools such as:
	  o **Magic**, **KLayout**, **Yosys**, **OpenROAD**, **Ngspice**, **Xschem**, **Netgen**, **GHDL**, **Verilator**, etc.
	• Develop and document exercises, assignments, and mini-projects for each design domain.
	• Record demos or work with AV teams to create training videos and tutorials.
	• Collaborate with content designers, platform developers, and trainers to align content with platform capabilities.
	• Test and validate open-source flows with actual design examples and student-level reproducibility.
	• Mentor junior engineers, interns, and trainers when needed.
	
	Preferred Skills
	• Prior teaching, curriculum development, or instructional design experience.
	• Exposure to cloud-based VLSI design environments or FPGA-based learning kits.
	• Knowledge of modern teaching aids – LMS platforms (e.g., Moodle), video content creation, screen recording tools.
	• Strong written and verbal communication skills.

6.Name of the Position	**Senior Trainers (VLSI Design)/ Senior VLSI Engineer**
Position Code	**2512-STVD**
No. of Position	**3**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs.65000/- P.M. 65000/- P.M
Eligibility Criteria and Experience	**Essential:** B.Tech/M.Tech in ECE, EE, VLSI Design or related field. **Experience**: 3 years of relevant experience in industry/academia/R&D Organization Note: Duration of PhD will be counted as R&D experience **Job description:** • To assist in design and development of reusable IP blocks using open-source EDA tools, their validation and documentation • To develop end-to-end ASIC/SoC design workflows using open-source EDA tools, and coordinate benchmarking of developed IPs and ASICs/SoCs against results from closed-source EDA tools to ensure performance, area, and power metrics are industry-comparable • Conduct Train-the-Trainer (ToT) programs for faculty and academic partners. • Deliver workshops, bootcamps, and webinars for students,

	faculty, and professionals. • Use open-source tools (e.g., Yosys, Magic, OpenROAD, KLayout, Ngspice, Verilator, Xschem) to conduct hands-on sessions. • Help participants with design challenges, practical labs, and capstone projects. • Serve as a point of contact for 10–20 assigned academic institutions. • Guide partner faculty in adopting and integrating course content into their curricula. • Provide ongoing academic mentorship and resolve technical or pedagogical queries. • Ensure learning continuity via LMS, forums, or online sessions. • Collect feedback, performance data, and learning outcomes. • Work with the central content and platform team to suggest improvements. • Assist in conducting assessments, certifications, and project evaluations. • Help users onboard and use the open-source chip design platform effectively. • Report technical issues and contribute to documentation and FAQs. • Maintain a knowledge base and support structure for learners and faculty.
7. Name of the Position	**DevOps Engineer**
Position Code	**2512-DOE**
No. of Position	**01**
Tenure/ Period	1 year (purely on contract basis with performance review every 3 months)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 65,000/- P.M
Eligibility Criteria and Experience	**Essential:** Bachelor's degree in Computer Science, IT, or related field (or equivalent experience). **Experience:**1 years of experience with cloud platforms and virtualization technologies. AWS experience is mandatory. **Job description:** Key responsibilities include: • Manage Kubernetes-based infrastructure on AWS EKS • Expertise in terraform or IAC tools. • Manage CI/CD pipelines for automated testing, building, and deployment gitlab/github action/harness. • Ensure high availability, reliability, and performance of services on production • Implement monitoring, logging, and alerting using tools like Prometheus, Grafana, ELK stack, or CloudWatch • Manage secrets, certificates, and access controls securely • Define and maintain infrastructure as code using Terraform or AWS CloudFormation • Optimize deployment processes, cost, and scalability across environmentsManage user authentication, data security, and access control mechanisms. • Set up storage solutions for lab files, simulation data, and course materials.

	• Collaborate with platform developers, instructional teams, and VLSI engineers to ensure infrastructure readiness. **Preferred Skills:** • Expertise in Kubernetes (EKS) cluster management and container orchestration • Strong knowledge of AWS services (EKS, EC2, RDS, S3, IAM, CloudWatch, etc.) • Proficiency in scripting (Bash, Python, or similar) • Experience with CI/CD tools (GitHub Actions, Jenkins, or similar) • Knowledge of Docker, Helm, and infrastructure monitoring tools along with AI tools. • Experience implementing security best practices (firewalls, IAM roles, VPC setups) Strong problem-solving and analytical skills. • Excellent communication and team collaboration abilities.
8. Name of the Position	**Full Stack Engineer**
Position Code	**2512-FSE**
No. of Position	**2**
Tenure/ Period	1 year (purely on contract basis with performance review every 3 months)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 65,000/- P.M
Eligibility Criteria and Experience	**Essential: -** • Bachelor's degree in Computer Science, IT, or related field (or equivalent experience). **Experience:** • 1 years of experience with full stack development preferably **LMS Developer** with hands-on experience in **Open edX** or similar open-source LMS platforms (Moodle, Canvas, Sakai). The ideal candidate will be responsible for end-to-end LMS setup, customization, integration, scaling, and ongoing maintenance to deliver a seamless learning experience to large user bases. **Job description:** Key responsibilities include: - Develop and maintain scalable web applications using Python, Django, Spring Boot, and React - Experience in front-end tools such as HTML, CSS, JS, React preferably for an LMS. - Integrate LMS with payment gateways, CRM, ERP, student portals, or mobile apps. - **Implement SSO using OAuth2, SAML, JWT, Azure AD, AWS IAM Identity Center, Keycloak.** - Develop custom XBlocks (Open edX), plugins, modules, extensions, or course components. - Configure learning paths, assessments, certificates, grading rules, and course structure. - Work with DevOps to ensure CI/CD and containerization best practices - Write unit and integration tests to ensure code quality - Perform code reviews and maintain high coding standards - Debug production issues and ensure platform uptime and performance - Integrate third-party tools such as Zoom, Teams,

	proctoring tools, analytics dashboards, etc. **Preferred Skills:** • Strong knowledge of Open edX architecture (LMS, Studio, XBlocks, APIs). • Experience with Python, Django, MySQL/PostgreSQL, REST APIs. • Familiarity with Docker, Kubernetes, Linux (Ubuntu), Nginx, Gunicorn/UWSGI, Redis. • Experience with AWS services: EC2, RDS, S3, CloudFront, EKS, IAM, VPC. • Experience with SCORM, xAPI (Tin Can), LTI is highly preferred. • Familiarity with Maven, REST APIs, Git, and CI/CD pipelines • Understanding of microservices and event architecture and containerized deployments (Docker/Kubernetes) • Experience working with cloud services on AWS
9. Name of the Position	**Resource Person (Admin and Account)**
Position Code	**2512-RP(AA)**
No. of Position	**1**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 50000/- P.M
Eligibility Criteria and Experience	**Essential: -** Graduate in any discipline **Experience:** Minimum 2 Years of experience in administrative/coordination roles specially in handling government project **Job Description:** • Looks up the admin and account related activities of the project • Assist the Program Head in day-to-day coordination of training, meetings, and project activities. • Maintain project documentation, reports, meeting minutes, and progress trackers. • Communicate with faculty coordinators, trainers, and institutional representatives as directed. • Follow up on tasks assigned to different teams and prepare brief status updates. • Help organize webinars, workshops, and outreach events by handling logistics and communication. • Support data entry and management of training records, feedback forms, and attendance. • Handle basic correspondence and email communications. • Ensure smooth internal coordination among content teams, platform developers, and trainers.
10. Name of the Position	**Assistant**
Position Code	**2512-Assistant**
No. of Position	**1**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 35 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 25000/- P.M
Eligibility Criteria and Experience	**Essential: -** Graduate in any discipline

	Experience: Minimum 1 Years of experience working as assistant **Job Description:** • Office Administration & Assistant Support: providing administrative assistance, managing day-to-day operations, and ensuring office efficiency. • File/Document Management: Managing physical and digital documents, including organization, storage, and retrieval. • Report Compilation & Data Entry: Compiling reports, entering data accurately, and maintaining records. • Meeting Coordination & Logistics: Planning, coordinating, and executing meetings, including logistics and communication. • Communication & Interdepartmental Liaison: collaborating effectively with various departments and Stakeholders
11. Name of the Position	**LMS Developer**
Position Code	**2512-LMSDEV**
No. of Position	**1**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 6 5,000/- P.M
Eligibility Criteria and Experience	**Essential:** Bachelor's degree in Computer Science, IT, or related field (or equivalent experience). **Experience:** 3+ years of experience consulting on LMS implementations. Experience with corporate L&D, universities, EdTech, or blended learning projects. Exposure to analytics dashboards (Superset, Power BI, Metabase).Background in instructional design or EdTech workflows (added advantage). **Scope of Work:** Planning, configuration, implementation, and optimization of our Learning Management System (Open edX / Moodle / Canvas / Totara or similar). The role is consulting-focused and involves requirement gathering, solution design, workflow creation, user onboarding, and coordinating with technical teams for enhancements. **Required Skills** • Strong understanding of LMS platforms: Open edX, Moodle, Canvas, Totara, Blackboard, etc. • Experience configuring courses, roles, certificates, assessments, and reports. • Knowledge of SCORM, xAPI/Tin Can, and LTI integrations. • Familiarity with SSO concepts (SAML/OIDC) and basic API-level understanding. • Ability to translate business needs into functional LMS solutions. **Key Responsibilities** 1. Requirement Gathering & Solution Design: • Conduct discovery sessions with stakeholders to understand training needs.

	• Recommend the right LMS features, workflows, integrations, and architecture options. • Create solution blueprints, course structures, learning paths, and user journeys. 2. LMS Setup & Configuration: • Configure LMS settings: roles, permissions, courses, catalogs, certificates, grading, user groups. • Set up learning programs, assessments, enrollments, notifications, and reporting. • Manage branding, theme settings, site configuration, and portal customization (non-code). **3. Integrations (Functional Oversight):** • Coordinate SSO integrations (SAML/OAuth2) with IT teams. • Oversee integrations with CRM/ERP/HRMS, payment gateways, Zoom/Teams, analytics, LTI tools. • Translate integration requirements into clear technical specifications for developers. **4. Content Strategy & Course Management** • Guide instructional teams in uploading SCORM, xAPI, video content, quizzes, and assignments. • Create templates for course authors and ensure content follows best practices. • Support content migration from legacy LMS systems. **5. Training, Documentation & Support:** • Conduct admin, instructor, and learner training sessions. • Create documentation, SOPs, onboarding guides, and LMS handbooks. • Provide L2 functional support and work with tech teams on bug reports or enhancements. **6. LMS Governance & Optimization:** • Audit LMS usability, performance, and workflows; recommend improvements. • Implement compliance and access policies across roles and departments. • Support release management, UAT, and version upgrades (functional testing).

General Terms & Conditions:

1. The qualification of candidates must be from Govt. University or Govt. recognized University/Institutions.
2. Applicants with last semester result awaited or incomplete degrees are not eligible to apply.
3. Cut-off date for calculating age and experience shall be the date mentioned in Walk-in-Interview Advertisement.
4. Non-refundable Registration Fee of ₹500/- per position to be deposited through online mode. The Candidates may deposit registration fee in the account of NIELIT in the given Bank account on or before Document Verification & Walk-in-Interview date.

Name of the office	National Institute of Electronics and Information Technology, New Delhi
Bank Account Number	604820100000012
Bank Name	Bank of India
IFSC Code	BKID0006048

Venue for Document Verification and Interview:	National Institute of Electronics & Information Technology, NIELIT Bhawan, Plot No. 3, PSP Pocket, Sector-8, Dwarka, New Delhi-110077
Document Verification	09:30 AM to 11:30 AM
Interview	11.00 A.M. onwards

5. Applications without requisite application fee (Rs. 500/-) shall be summarily rejected at any stage of Document Verification and Walk-in-Interview.
6. Applicants are requested to fill Application Form and attach all the required (self-certified) documents including Payment Receipt.
7. The Applicants who report at NIELIT HQ before 11:30 AM shall be considered for Document Verification.
8. Applicants are requested to come with Original Documents for Document Verification.
9. Document Verification (based on the documents produce by applicant with application form) and Walk-in Interview is to be done as per date mentioned in the advertisement.
10. Only those candidates who clears Document Verification will be allowed to appear in Walk-in-Interview.
11. Applicants are requested not to send Application Form thru Post or any other medium to NIELIT HQ.
12. NIELIT has the right to accept or reject the application without assigning any reason thereof.
13. Applicants are advised to visit the website of NIELIT **http://nielit.gov.in/recruitments** for any updates.
14. No separate communication shall be made in any other form.
15. The number of vacancy is tentative and liable to change as per the requirement of NIELIT.
16. The Remuneration mentioned above is consolidated salary (CTC). The selected candidate will not be paid any other financial benefits like Medical, HRA, Transport etc. except the consolidated salary.
17. Selection of candidate for appointment to the above mentioned position will be based on the performance of the candidates in the walk-in-interview and as found eligible as per prescribed criteria.
18. The selected candidate will be engaged purely on contract basis initially for a period of one year, which may be extended depending upon the requirement and performance of the candidate.
19. The offer of appointment for the selected candidate will be subject to verification of original certificates/testimonials at the time of interview and completeness of other formalities.
20. NIELIT will also create a panel for contractual deployment and the candidates will be selected for deployment on contract from the panel as and when required.
21. Only those candidates who deposit requisite registration fee of Rs. 500/-, clear document verification and successful interaction will be empaneled.
22. Empanelment means the shortlisted candidates will be in the panel of NIELIT for one year. They may be deployed in specific Govt. department/ NIELIT as per department requirements purely on contract basis. Mere empanelment does not ensure deployment in any department nor provide any right to candidate to claim for deployment.
23. Empaneled candidates list will valid for one year from the date of result declaration.
24. Candidates will not be entitled to claim any TA/DA for appearing in Interview.
25. Canvassing/trying to influence NIELIT employees to secure the job in any manner shall disqualify the candidate.
26. The applicants applying for the contractual position of Consultant- DFT and FPGA Validation) and Consultant (Physical Design) are required to sign an Agreement at the time of joining
27. In the case of any legal dispute, the jurisdiction shall be Delhi.